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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

SAR WITH PARTIAL CAPACITOR SAMPLING TO REDUCE PARASITIC CAPACITANCE

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention pertains in general to data converters and, more particularly, to analog-to-digital converters utilizing a charge-redistribution, binary-weighted switched-capacitor array.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] This application is Continuation-in-Part of US Patent Application Serial Number 10/453,369, is now a U.S. Patent 6,882,298
filed June 3, 2003, and entitled "SAR ANALOG-TO-DIGITAL CONVERTER WITH TWO SINGLE ENDED INPUTS," Atty. Dkt. No. CYGL-26248, and is related to pending application entitled "NOISE CANCELLATION IN A SINGLE ENDED SAR CONVERTER," Atty. Dkt. No. CYGL-26,543; and pending application entitled "SAR DATA CONVERTER WITH UNEQUAL CLOCK PULSES FOR MSBS TO ALLOW FOR SETTLING," Atty. Dkt. No. CYGL-26,545; and pending application entitled "HIGH SPEED COMPARATOR WITH BLOCKING SWITCHES FOR SAR CONVERTER," Atty. Dkt. No. CYGL-26,550; and pending application entitled "COMMON CENTROID LAYOUT FOR PARALLEL RESISTORS IN AN AMPLIFIER WITH MATCHED AC PERFORMANCE," Atty. Dkt. No. CYGL-26,552," and pending application entitled entitled "OPEN LOOP COMMON MODE